REMARKS

Claims 6-7 and 9-11 are pending in this application. Claims 6-7 and 9-11 are rejected under the provisions of 35 U.S.C. 103(a).

Applicants have amended claims 6, 9, and 11. Claim 6 has been amended to include the limitations of claim 7. Claim 7 has been cancelled. Claim 9 has been amended to adjust the dependencies. Claim 11 has been amended to appear in independent form. Applicants note that a typographical error had resulted in claim 11 recited to be dependent from claim 1, which had previously been cancelled. Applicants believe that the Examiner understood claim 11 to depend from independent claim 6. No new matter has been added. Therefore, applicants respectfully request that the Examiner enter the after final amendments.

Applicants acknowledge the courtesy and cooperation of the examiner in participating in a telephonic conference on or about October 8, 2002, to discuss the pending application. The Examiner has rejected claims 6-7 and 9-11 under 35 U.S.C. §103 as unpatentable over the combination of A. McTeer, U.S. Patent No. 5,939,788 (McTeer) and K. Robinson et al., U.S. Patent No. 6,054,172 (Robinson). During the interview the claims and cited prior art references were discussed with no agreement reached.

In accordance with the discussion presented below, applicants believe that the claims in their present form are allowable and distinguishable from the cited prior art references.

The claim 6 limitation that "the same mask used to pattern the dielectric layer is used to pattern the aluminum" was indicated by the Examiner to be anticipated by McTerr (FIGS. 1-5, col. 18 lines 15-25 and claim 7). Close examination of these drawings indicates that these drawings do not indicate a sequence of steps but instead refer to alternative embodiments. See Brief description of drawings at 14:33-67. The portion of the specification in McTeer referenced by the examiner (18: 18-19) merely provides a detailed description of FIG. 2.

As is evident from FIG. 2, a conformal copper diffusion barrier 4 is deposited prior to an aluminum wetting layer 5. But the copper diffusion barrier layer is not copper but "may be any metal nitride, and includes tantalum nitride, titanium nitride, tungsten nitride and titanium

aluminum nitride. (18: 10-13). Thus, if FIG. 2 is interpreted consistently with MCTeer's teachings as to the damascene process, McTeer inherently teaches the use of a mask to create only the opening in the insulator layer 1 shown in FIG. 2. There is no teaching or suggestion that such a mask is used to pattern any other layers, let alone an aluminum layer. Instead, McTeer teaches the use of a mask on only one occasion, at the time of formation of the opening in the insulator layer 1. Moreover, the sequence of steps recited in the claims requires the same mask to be used at least twice, i.e., before filling with copper and after filling with copper (and depositing aluminum). FIG. 2 shows no use of a mask after depositing aluminum, hence can't teach the use of a mask to pattern and etch the aluminum as recited in claim 6.

Claim 7 of McTeer also fails to teach or suggest the claimed limitation. Claim 7 indicates that the second insulating layer is patterned to form a patterned second insulating layer having an opening wherein the opening lies over at least part of the conductive metal plug. This portion fails to teach or suggest the opening coincident with the opening used for the plug, let alone the same mask used to form both. Moreover, the second opening is not a "patterning and etching" of aluminum, but instead refers to a patterning of an insulator. Applicant recognizes that the examiner has attempted to use the combination of McTeer and Robinson to show that patterning and etching of aluminum is obvious, but even if the two references are used, none of them shows a limitation of the same mask being used twice. For at least these reasons, applicant submits that the combination of McTeer and Robinson fails to teach or suggest all of the limitations of claim 6. The examiner is respectfully requested to reconsider his rejection and to review and reconsider the cited portions of McTeer.

Claim 11 has been amended to appear in independent form, adopting the limitations of base claim 6. Previously, claim 11 was in dependent form and mistakenly listed as dependant from claim 1 (previously cancelled). Therefore applicants submit that no new matter has been added. Claim 10 depends from claim 11. Applicants submit that both claims 10 and 11 are in allowable form, for at least the reason that the combination of McTeer and Robinson fail to teach or suggest " patterning and etching the aluminum so that the aluminum overlies only areas filled with copper" and copper thickness within the range of 0.3 to 3.0 microns and aluminum with a

thickness in the range of 0.5 to 3.0 microns. The examiner rejected the claim based on McTeer col.2, lines 60 and claim 26. (See office action, page 3). But neither of those dimensions in the reference relate to a thickness of either aluminum or copper. Instead McTeer teaches (with reference to FIG. 14), an aluminum **diffusion barrier** layer 18 made up of typically titanium or titanium nitride (see text language , 22:56-60) and a copper **diffusion barrier** layer (see claim 26). As explained by McTeer (18:15-20) , a copper diffusion barrier layer 4 may be any metal nitride and includes tantalum nitride, titanium nitride, tungsten nitride, etc. There is no teaching or suggestion that it contains copper, but rather the opposite that it prevents diffusion of copper layers. Hence, neither McTeer nor Robinson teach aluminum or copper layers (distinguished from aluminum and copper diffusion barrier layers) having the thicknesses recited in the claims.

Further, as to dependant claim 10, none of the cited prior art references teaches the additional limitation "wherein the thickness of the copper and the thickness of the aluminum are adjusted so that the completed interconnect line has a first predefined electrical resistance within the range of 0.012 to 0.008 Ω per unit length." The examiner on page 5 of the office action rejected claim 10 based on McTeer 1: 39-45 and 18:60-65). But McTeer at that location only teaches forming a silicide to obtain low resistance and further teaches that the industry has migrated to investigating copper as a more conductive metal compared to aluminum. McTeer is silent as to selecting thickness of copper and aluminum and adjusting the thickness of both to meet the resistance characteristics in the ranges recited in the claims. Thus, for at least this reason, McTeer in combination with Robinson fails to teach the elements of claim 10.

Conclusion

Accordingly, it is submitted that all issues in the Office Action have been addressed, and withdrawal of the rejections is respectfully requested. Applicants believe that this application is in condition for allowance, and respectfully request a prompt passage to issuance. If the Examiner believes that a telephone conference would expedite the prosecution of this application, he is invited to contact the Applicants' undersigned attorney at the telephone number set out below.

Respectfully submitted,
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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

(Includes All pending Claims)

CLAIMS

We Claim:

6. (Twice Amended) A method for fabricating low resistance interconnect lines in an integrated circuit, the method comprising the steps of:

patterning and etching a dielectric layer in an integrated circuit;

filling the etched areas of the dielectric layer with copper;

depositing aluminum on the copper;

patterning and etching the aluminum so that the aluminum overlies only areas filled with copper, wherein the same mask used to pattern the dielectric layer is used to pattern the aluminum.

7. Cancelled, without prejudice.

9. (Twice Amended) The method of claim [7] 6 wherein a barrier material is deposited atop the copper before the aluminum is deposited and patterned.

10. The method of claim 11 wherein the thickness of the copper and the thickness of the aluminum are adjusted so that the completed interconnect line has a first predefined electrical resistance within the range of 0.012 to 0.008 Ω per unit length.

11. (Once amended) A method for fabricating low resistance interconnect lines in an integrated circuit, the method comprising the steps of:

patterning and etching a dielectric layer in an integrated circuit;

filling the etched areas of the dielectric layer with copper;

depositing aluminum on the copper;

patterning and etching the aluminum so that the aluminum overlies only areas filled with copper, [The method of claim 1] wherein the copper has a thickness within the range of 0.3 to 2.0 μm and the aluminum has a thickness within the range of 0.5 [microns] to 3.0 μm.